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PDUXB 2.22.5

Main code release notes

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NOTE THAT 2-22-X FIRMWARE REQUIRES NEWER PDUXSETUP THAN 2-21-X. PLEASE ENSURE YOU INSTALL THE LATEST PC SUITE FROM OUR WEBSITE. Note also that an optimisation in the new PduXSetup liberates additional schematic logic space in 2-21-x and 2-20-x firmware calibrations, but older PduXSetup versions will not be able to load and program those calibrations (or monitor them once programmed) since they do not understand the optimisation.

Power Config:

* Power configuration format has been raised from 1 to 2, now including settings for maximum wake duration on inputs 13/14/15/16 (PDUX3/4/6B) and inputs 9/10/11/12 (PDUX2B).

Because of the format change, the power configuration will be set to default in any unit when you program the new firmware (or indeed go backwards from the new firmware to older firmware). You should save the power configuration before programming the new firmware. Then start by getting the default new-format power configuration from a unit after programming with the new firmware and a blank new calibration. You may then edit the format number and insert the four additional settings lines using notepad or anything similar as required to convert older configuration files.

This change was made in particular to allow for timeouts on wake from things like door switches. If the wake from a particular pin times out in this way (and is the only source of wake at that time) the device will sleep, and will not wake again from that source until it validates to inactive first (ie you would have to close and re-open the door to wake again).

Expanded logical component and compute budgets:

- * Increased PDUX2/3/4/6B logic components supported from 512(all) to 512/768/1024/2048 respectively
- * Increased PDUX2/3/4/6B compute budgets to match increased logic (maximum number of components, all at 100Hz)

This is a significant change in the quantity of logic that you can create, especially for PDUX4B and PDUX6B, and even more so when combined with the changes below and the additional internal optimisations in PduXSetup.

Component input inversion:

- * Optional inversion at the input for most logic component boolean inputs

Almost all boolean component inputs are now capable of inversion at the component, meaning that almost everywhere that you would have needed an INVERT component before, you no longer need one. Hover the mouse cursor over the attachment point for the input and right-click to see the "invert" toggle option. When inverting, the component input will display an inversion circle. This applies to AND/OR/XOR but also to the inputs on many other components such as FLASH and COUNTER components, and things like the clock/set/reset inputs to a FLIPFLOP or LATCH and so on.

Additional logic component inputs:

- * AND/OR/XOR now up to 8 inputs
- * ADD/MIN/MAX now up to 8 inputs

New logic components:

- * Added dynamic flash component (flash times are inputs, similar to dynamic delay)
- * Added accumulator component for integrators etc (gain, min, max, optional reset, optional set, set-value)

This component was added in particular to ease creating simple I (or indeed PI or PID) controllers. It is now possible to make a complete PID controller with just 8 components (plus a few constant values). See attached example of a simple PI with integral windup prevention.

- * Added dynamic recursive filter component (filter constant 0-1 is input)

For example a fuel-level sensor should be very heavily filtered when the vehicle is moving, but hardly filtered at all when the vehicle is stopped (and could be subject to re-fuelling).

- * Added recursive filter component with fixed constant plus a not-filtered initialisation time

The initialisation time allows the filter to immediately adopt the value of a sensor at power on before the filtering cuts in.

- * Added range-limit (clip) component with min and max as inputs
- * Added range-limit (clip) component with fixed min and max

In many instances one wants to limit both min and max of a value, so this makes the process simpler and clearer.

- * Integer counters gain an optional set input with fixed set value
- * Integer counters allow negative values, minimum is configurable, range increases to +/-1000000

- * Fixed delay component range increases to 1000000s and resolution increases to 0.001s
- * Fixed flash component range increases to 1000000s and resolution increases to 0.001s
- * Latch auto-cancel range increases to 1000000s and resolution increases to 0.001s

- * Added hysteresis to equal/not-equal in addition to margin

This is designed for easily recognising voltages ranges from a resistor/switch network where multiple driver input switches drive a single PDU input pin. Compare the input voltage as equal to the nominal switch-active voltage with a margin for tolerances, plus a hysteresis for stability. Ideally then add a delay component with (eg) 100ms on and 100ms off times as a validation component to create a clean signal for the rest of the logic to use.

Miscellaneous:

- * Warning if main calibration CAN1 termination setting does not match power configuration CAN1 termination setting
- * A fix to non-zero hysteresis for < and > with integer-values
- * Prevented triggering of edge-triggered counters on first service in unusual circumstances
- * Power config text labels for PDUX2B optional wake pins have been corrected
- * You can now monitor the 5V sensor supply output voltage via a new QTY